MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2017/2018

EEN1046 – ELECTRONICS III
(TE, RE, BE)

6 MARCH 2018
2:30 p.m. - 4:30 p.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

(a) This booklet consists of 6 pages including cover pages with 4 questions only.

(b) Attempt **ALL** questions given. All questions carry equal marks and distribution of the marks for each question is given.

(c) Please write all your answers in the Answer Booklet provided.

(d) All necessary working **MUST** be shown.

Question 1

(a) Sketch a symbol diagram of an op-amp and name all the input/output ports.

[5 marks]

(b) Given the op-amp configuration in Figure Q1 (b) below, determine the value of R_f required to produce a closed loop voltage gain of –150. What type (inverting or non- inverting) of op-amp is this?

[5 marks]

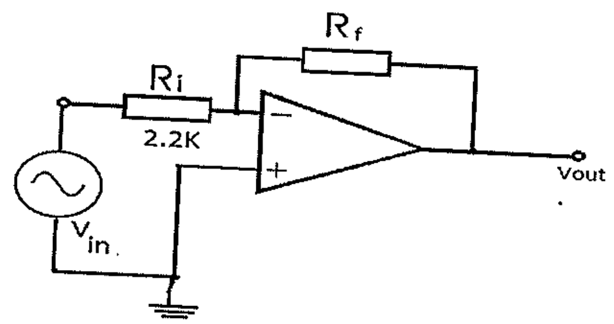

Figure Q1 (b)

(c) Given the summing amplifier in Figure Q1 (c) with $R_F = 20$ kΩ, $R_1 = 2$ kΩ, $R_2 = 4$ kΩ, and $R_3 = 6$ kΩ.

(i) Determine the type (inverting or non-inverting) of the summing amplifier in Figure Q1 (c) and justify your answer.

[2 marks]

(ii) Express the output voltage, v_o, in terms of v_{I1}, v_{I2}, and v_{I3}.

[6 marks]

(iii) Determine the output voltage, v_o, given the v_{I1} is 2 V, v_{I2} is 4 V, and $v_{I3} = 6$ V.

[3 marks]

(iv) Modify the circuit components values so that the summing amplifier in Figure Q1 (c) gives $v_o = -(v_{I1} + v_{I2} + v_{I3})$.

[4 marks]

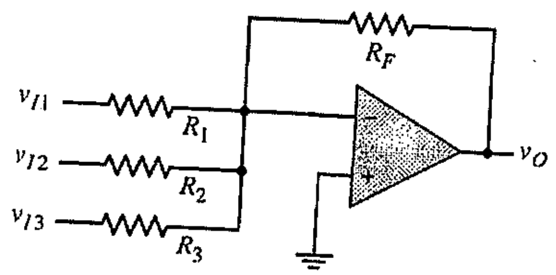

Figure Q1 (c)

Continued ...

Question 2

(a) Figure Q2 (a) shows a Band-Pass filter circuit with constant pass-band gains. Given $R_1=R_1'=R_F=R_F'=10k\Omega$, $C=10nF$, $R=10\ k\Omega$, $C'=5nF$, $R'=12k\Omega$ and Bandwidth, BW =1 kHz.

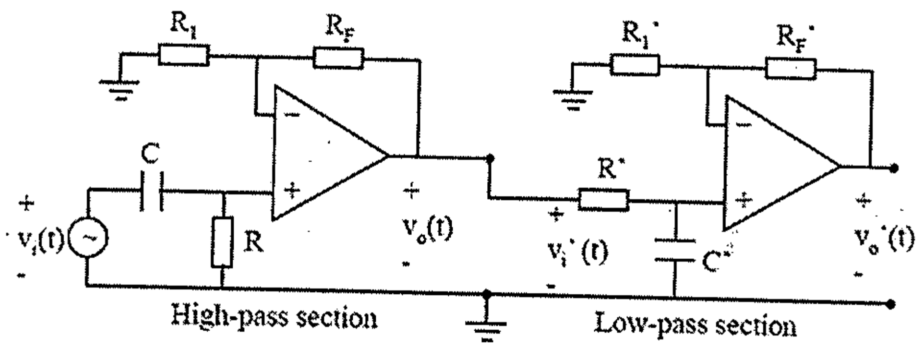

Figure Q2 (a)

(i) Calculate the high pass gain, K_{HP} and low pass gain, K_{LP}.

[2 marks]

(ii) Calculate the overall band pass gain, K_{BP}.

[2 marks]

(iii) Calculate the highest cutoff frequency, f_H and lower cutoff frequency, f_L.

[2 marks]

(iv) Calculate the quality factor Q.

[2 marks]

(b) The Darlington-pass transistor regulator circuit shown in Figure Q2 (b) regulates the output voltage to 5V. Given that the transistor current gain for Q1 and Q2 are 100 and $V_{BE} = 0.7V$.

(i) Determine the total Darlington-pair current gain, h_{FE}

[1 mark]

(ii) Calculate the Zener voltage, V_Z and Zener current I_Z.

[6 marks]

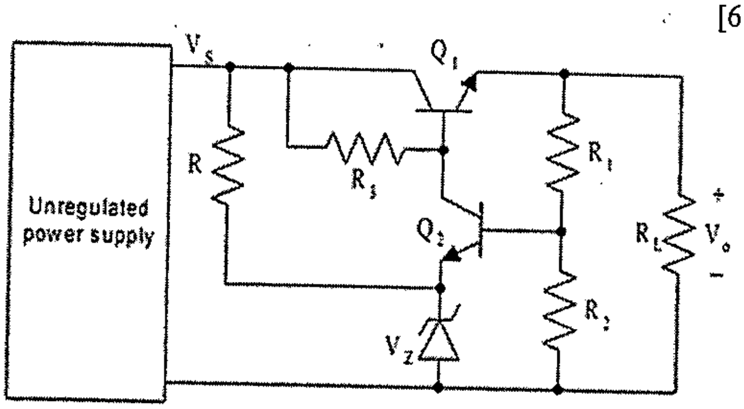

Figure Q2 (b)

Continued ...

(c)

(i) What is the difference between sawtooth and triangular waveforms?

[2 marks]

(ii) Design a triangular wave generator, as shown in Figure Q2 (c), for an amplitude voltage of ±10V and oscillation frequency of 10KHz. Assume $V_{CC} = \pm 15V$, C=1nF. Assume R_1= 1KΩ.

[6 marks]

(iii) Modify the circuit to produce a sawtooth waveform instead of triangular waveform.

[2 marks]

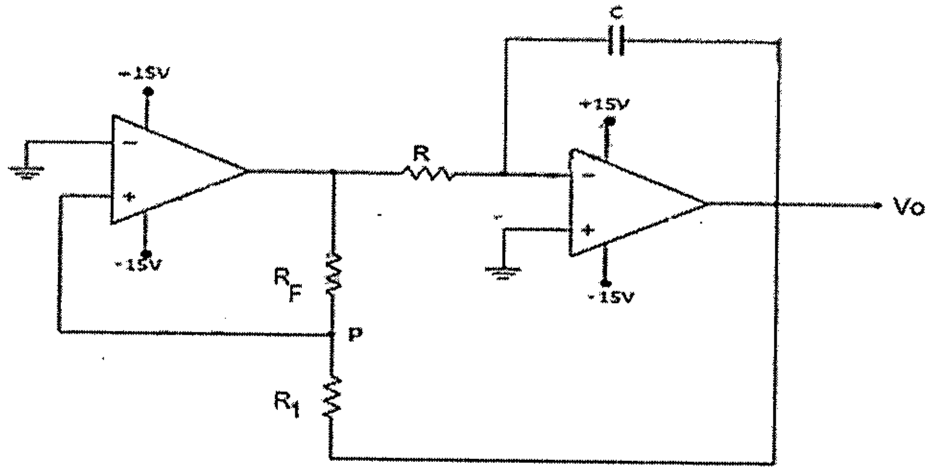

Figure Q2 (c)

Question 3

(a) The op-amp in Figure Q3 has the following property obtained from datasheet:

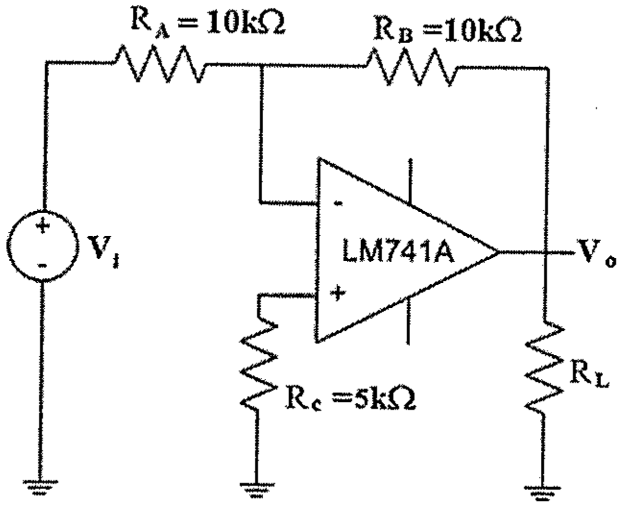

Figure Q3

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Parameters	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$T_A = 25^0C$		1.0	3.0	mV
Input Offset Current	$T_A = 25^0C$		3.0	30	nA
Input Bias Current	$T_A = 25^0C$		15	80	nA
Input offset voltage drift coefficient	D_v			15	$\mu V/^0C$
Input offset current drift coefficient	D_i			0.5	$nA/^0C$
Input bias current drift coefficient	D_b			0.5	$nA/^0C$
Power Supply Rejection Ratio	PSRR	75	85		dB

(i) Determine the drift output offset voltage of the circuit in Figure Q3 at temperature $T = 45°C$.

[7 marks]

(ii) Determine maximum output offset voltage due to V_{IO}, for an operating temperature of 45°C. Assuming $I_{IO} = I_B = 0$.

[3 marks]

(iii) Determine the maximum output offset voltage due to V_{IO}, at room temperature (25°C). Assuming $I_{IO} = I_B = 0$.

[3 marks]

(iv) Determine the maximum output offset voltage, taking into account the effect of all the relevant dc offset value, for an operating temperature of 45°C.

[3 marks]

(b) Stability is a very important consideration when using op-amps. Discuss the stability in op-amp while performing positive feedback and negative feedback respectively.

[9 marks]

Question 4

(a) A temperature sensor senses a temperature ranging from 0° to 20°C and output a corresponding voltage of from -5V to +5V. The output voltage linearly increases with the temperature sensed. Design a Schmitt trigger circuit that will turn on a heater (Schmitt trigger output = $+V_{sat}$) when the temperature drops below 5 °C and turn off the heater (Schmitt trigger output = $-V_{sat}$) when temperature rises above 15°C. Assume supply voltage $V_{cc} = \pm 12V$ and $V_{sat} = V_{cc} - 1$. Assume diode voltage of 0.7 V in your design.

(i) What type of Schmitt trigger circuit is required in this sensing circuit? Justify your answer.

[2 marks]

(ii) Sketch and label the Schmitt trigger circuit.

[3 marks]

(iii) Sketch the output of the Schmitt trigger circuit in relation to the sensing input of the temperature sensor.

[3 marks]

(iv) Evaluate the analysis on the design in order to determine the resistive components values required for the Schmitt trigger circuit.

[5 marks]

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(b) Assuming an ideal diode D as shown in Figure Q4 (b), a voltage V_{in} is connected to the inverting input of a precision clamper circuit.

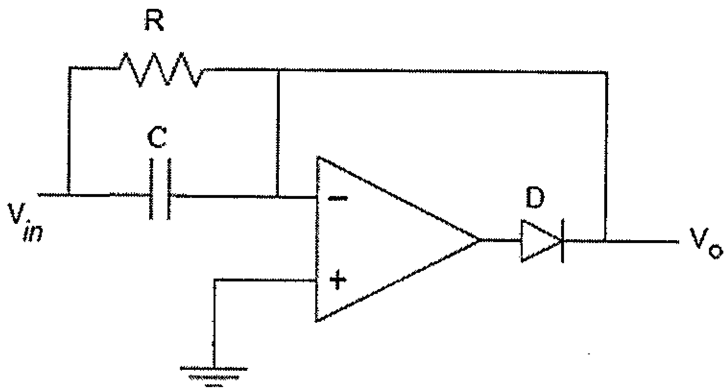

Figure Q4 (b)

(i) If the input voltage $V_{in} = V_m \sin\omega t$, explain briefly the operation of the circuit and evaluate the output voltage, V_o from 0 to 2π time intervals.

[7 marks]

(ii) The input voltage, $V_{in} = 2 \sin\omega t$ is to be clamped to a DC level of +8V. Assuming an ideal op-amp and ±12V supply voltage, modify the circuit in Figure Q4 (b) to obtain the required output.

[5 marks]

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